ABSTRACT OF THE DISCLOSURE

A ferroelectric memory device having a multi-layer electrode structure and a fabricating method thereof are described. The ferroelectric memory device includes a semiconductor substrate having first and second transistors, an interlayer insulating layer covering the first and second transistors, and first and second ferroelectric capacitor sequentially stacked on the interlayer insulating layer. The first ferroelectric capacitor includes a lower electrode, a first ferroelectric layer, and a middle electrode sequentially stacked on the interlayer insulating layer, while the second ferroelectric capacitor includes the middle electrode, and a second ferroelectric layer and an upper electrode sequentially stacked on the middle electrode. First and second transistors are selectively connected to the first and second ferroelectric capacitors, respectively, forming two or one unit cell. Therefore, it is possible to form a unit cell in a smaller area than a conventional area, and increase an area that a capacitor occupies.